Docket No.: 42390.P4049R

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	)	
	)	
William S. Wu et al.	)	
	)	
Serial No.: not yet assigned	)	Examiner: not yet assigned
Reissue of US Patent 5,961,621	)	
	)	
Filed: herewith	)	Art Unit: not yet assigned
	)	
For: MECHANISM FOR EFFICIENTLY PROCESSING DEFERRED ORDER-DEPENDENT MEMORY ACCESS TRANSACTIONS IN A PIPELINED SYSTEM	)	

Reissue Application

Hon. Commissioner of
Patent & Trademarks
Washington, D.C. 20231

Dear Sir:

Applicants respectfully request entry of the following amendment and consideration of the following remarks.

IN THE CLAIMS

Please add the following new claims.

10. (New) An apparatus comprising:

a chipset to receive a first ordered transaction and to generate a defer signal and a visibility signal indicating when a second ordered transaction can be issued before the first ordered transaction is complete.

11. (New) The apparatus of claim 10 further comprising

an agent coupled to the chipset, wherein the agent is configured to: issue the first ordered transaction, defer processing the first ordered transaction in response to the defer signal, and issue a second ordered transaction in response to the visibility signal before the first ordered transaction is complete.

12. (New) An apparatus comprising:

an agent configured to: issue a first ordered transaction, receive a defer signal and a visibility signal, and issue the second ordered transaction in response to the defer signal and the visibility signal before the first ordered transaction is complete.

13. (New) The apparatus of claim 12, the agent further configured to:

defer processing of the first ordered transaction in response to the defer signal.

14. (New) The apparatus of claim 13 further comprising:

a chipset to receive the first ordered transaction and to generate the defer signal and the visibility signal.

15. (New) The apparatus of claim 11 or claim 13 wherein the agent postpones the second ordered transaction if the defer signal is asserted and the visibility signal is negated.

16. (New) The apparatus of claim 11 or claim 13 wherein the agent issues the second transaction if the defer signal is asserted and the visibility signal is asserted.

17. (New) A method for processing order-dependent memory access transactions comprising:

issuing a first ordered transaction;

receiving a defer signal;

deferring processing of the first ordered transaction responsive to the defer signal;

receiving a visibility signal; and

issuing a second ordered transaction responsive to the visibility signal before the first ordered transaction is completed.

18. (New) The method of claim 17 further comprising:

postponing the second ordered transaction if the visibility signal is negated.

19. (New) A method for processing order-dependent memory access transactions comprising:

receiving a first ordered transaction;

generating a defer signal to defer processing of the first ordered transaction;

generating a visibility signal to indicate when a second ordered transaction can be issued before the first ordered transaction is completed; and

receiving the second ordered transaction.

20. (New) The method of claim 19, the visibility signal being generated also to postpone the second ordered transaction when the visibility signal is negated.

21. (New) The method of claim 17 or of claim 19 further comprising:

stalling the first ordered transaction if the first ordered transaction is not ready.

22. (New) The method of claim 17 or of claim 19 further comprising:

accessing a cache line in a cache memory if the cache line is one of the clean, shared, and modified states.

23. (New) The method of claim 21 further comprising:

postponing the second ordered transaction until the first ordered transaction is complete.

24. (New) The method of claim 22 further comprising:

completing the first ordered transaction.

25. (New) A computer system comprising:

a bus interface; and

a chipset to receive a first ordered transaction on the bus interface and to generate a defer signal and a visibility signal responsive to receiving the first ordered transaction when a second ordered transaction can be issued before the first ordered transaction is completed.

26. (New) The system of claim 25 wherein the defer signal is asserted and the visibility signal is negated to postpone a second ordered transaction.

27. (New) The computer system of claim 25 further comprising:

an agent coupled to the chipset to: issue the first ordered transaction, defer processing the first ordered transaction in response to the defer signal, and issue the second ordered transaction in response to the visibility signal before the first ordered transaction is complete.

28. (New) The system of claim 27 wherein the defer signal is asserted and the visibility signal is asserted to cause the agent to issue the second ordered transaction before the first ordered transaction is complete.

REMARKS

Error

Applicants submit that the differences in scope in many of applicants' new independent claims in the present reissue application are primarily that the claims cover an "apparatus" (and its corresponding method) instead of a "system" (and its corresponding method). Applicant believes that the claims here presented contain the salient limitations required for patentability in the original case.

At the time of the original case, however, applicants' attorneys made an error in legal judgment. Applicants' attorneys thought that only system-level claims should be pursued based on what is now believed to be a misunderstanding of the relatively fluid and unclear area of the law pertaining to implied licenses and patent exhaustion. This was a "mistake" as defined under the re-issue statutes because the attorneys failed claim the certain aspects of the invention. In particular, applicants' attorneys failed to claim the invention at the "apparatus" level.

Notably, some claims are described as "system" claims for convenience only. That is, the claims are limited only by their own limitations. The claims currently read on some system level implementations as they recite a bus (or alternatively some recite "system" in the preamble). Such buses may in some embodiments be integrated into a single bus agent or other device. The claims existing prior to this reissue are not limited to being buses that are separate from a bus agent or apparatus of any sort. In other words,

they may be integrated into an integrated circuit or bus agent in some cases.

Applicants believe that in at least some if not all cases, the form factor or the connection to a bus are not crucial to the inventive aspects of the inventions claimed in applicants' claims. Thus, applicants' new claims are drafted to devices such as integrated controller circuits or individual bus agents regardless of whether they are connected by a bus. That is, an interface to connect to a bus may be present, but the device itself is covered by the claims whether or not it is connected to a bus (internal or external to the device).

Status of Claims under 37 CFR § 1.173(c)

Claims 1-9 stand as issued claims and remain in their unamended state.

Claims 10-28 are newly presented claims for examination.

Explanation of support under 37 CFR § 1.173(c)

Applicants' newly presented independent claims in many cases closely mirror the claims previously allowed, only in apparatus format, as illustrated by the table below:

New Claim	Support from Claim
10	7 (chipset)
12	7 (agent)
17	1 (agent method)
19	1 (chipset method)
25	7 (system comprising chipset)

Support for most of the dependent claims here presented may be readily found in independent and dependent claims in the original patent (5,961,621). Support is also

present in the patent specification as well.

Conclusion

Applicant submits that these amendments do not add new matter and that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: 10-3-01

Jeffrey S. Draeger, Reg. No. 41,000

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8598

"Express Mail" mailing label number: EL617209823US

Date of Deposit: October 4, 2001

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Conny Willesen

(Typed or printed name of person mailing paper or fee)

Conny Willesen

(Signature of person mailing paper or fee)

10-4-01

(Date signed)